# 2Mx32 (5V Supply; 5V or 12V Program) FLASH MODULE   *PRELIMINARY**

FEATURES

- Maximum Access Time of 100ns
- Packaging
  - 68 Lead, Plastic PLCC, 24.71 mm (0.973 inch) square
- Sector Architecture
  - 32 equal size Blocks of 64KBytes per each 2Mx8 chip
- Minimum 100,000 Write/Erase Cycles
- Organized as 2Mx32
- Commercial and Industrial Temperature Ranges
- 5V Vcc/5V or 12V VPP

- Low Power CMOS, 0.5mA Standby Typical
- Automated Programs and Block Erase
  - Command User Interface
  - Status Register
- Automated Suspend Options
- Hardware $\overline{RESET}$ Pin

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

FIG. 1   PIN CONFIGURATION FOR WPF2M32-100PJX

TOP VIEW
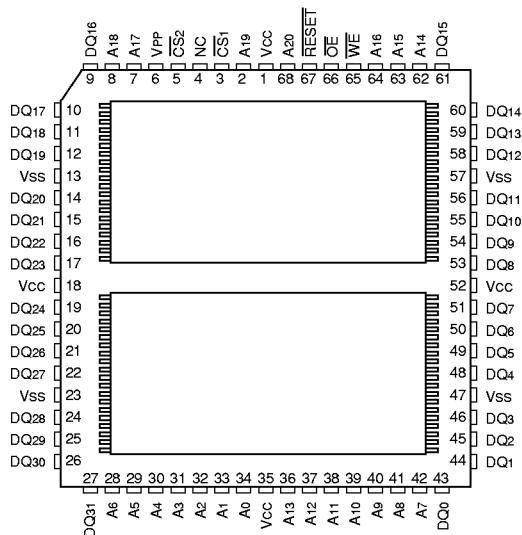
PIN DESCRIPTION

DQ0-31	Data Inputs/Outputs
A0-20	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-2}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{RESET}$	Reset
Vcc	Power Supply
VPP	Programming Voltage
Vss	Ground
NC	No Connect

BLOCK DIAGRAM
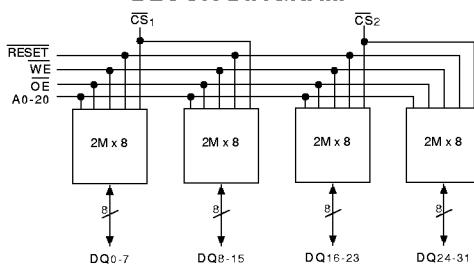
ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature (Com)	0 to +70	°C
Operating Temperature (Ind.)	-40 to +85	°C
Supply Voltage Range (Vcc)	-2.0 to +7.0	V
Signal Voltage Range (any pin except VPP and $\overline{\text{RESET}}$) (2)	-2.0 to +7.0	V
Storage Temperature Range	-55 to +125	°C
Endurance (write/erase cycles)	100,000 cycles min.	
VPP and $\overline{\text{RESET}}$ Voltage (3)	-2.0 to +14.0	V

NOTES:

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V and -0.2V on Vcc, $\overline{\text{RESET}}$, and VPP. During voltage transitions, inputs may overshoot Vss to -2.0V for periods of up to 20ns. Maximum DC voltage on input and I/O pins is Vcc + 0.5V. During voltage transitions, input and I/O pins may overshoot to Vcc + 2.0V for periods up to 20ns.
3. Maximum DC input voltage on VPP and $\overline{\text{RESET}}$ which may overshoot to 14.0V for periods up to 20ns.
4. **Recommended soldering temperature not to exceed 215°C for 20 seconds.**

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	4.5	5.5	V
Input High Voltage	VIH	2.0	Vcc + 0.5	V
Input Low Voltage	VIL	-0.5	+0.8	V
Operating Temp. (Com)	TA	0	+70	°C
Operating Temp. (Ind)	TA	-40	+85	°C

CAPACITANCE
(TA = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{\text{OE}}$ capacitance	COE	VIN = 0 V, f = 1.0 MHz	50	pF
$\overline{\text{WE}}$	CWE	VIN = 0 V, f = 1.0 MHz	50	pF
$\overline{\text{CS}}_{1\text{-}4}$ capacitance	CCS	VIN = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	CI/O	VI/O = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	CAD	VIN = 0 V, f = 1.0 MHz	50	pF
$\overline{\text{RESET}}$	CRST	VIN = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(Vcc = 5.0V ± 0.5V, TA = -40°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Input Load Current (V$_{IN}$ = V$_{SS}$ or V$_{CC}$, V$_{CC}$ = V$_{CC}$ Max)	I$_{LI}$			4	μA	1
Output Leakage Current (V$_{OUT}$ = V$_{SS}$ to V$_{CC}$, V$_{CC}$ = V$_{CC}$ Max)	I$_{LO}$			40	μA	1
V$_{CC}$ Standby Current　　　　　(V$_{CC}$ = V$_{CC}$ Max, $\overline{CS}$ = V$_{CC}$ ±0.2V) 　　　　　　　　　　　　　　(V$_{CC}$ = V$_{CC}$ Max, $\overline{CS}$ = V$_{IH}$)	I$_{CCS}$		100 1.6	400 8	μA mA	1,3,6
V$_{CC}$ Read Current ($\overline{CS}$ = V$_{IL}$, $\overline{OE}$ = V$_{IH}$, f = 8MHz, I$_{OUT}$ = 0mA, CMOS inputs)	I$_{CCR1}$		68	140	mA	1,5,6
V$_{CC}$ Read Current ($\overline{CS}$ = V$_{IL}$, $\overline{OE}$ = V$_{IH}$, f = 8MHz, I$_{OUT}$ = 0mA, TTL inputs)	I$_{CCR2}$		80	200	mA	1,5,6
V$_{CC}$ Write Current (Word Write in Progress)	I$_{CCW}$			140	mA	1,7
V$_{CC}$ Block Erase Current (Block Erase in Progress)	I$_{CCE}$			120	mA	1,7
V$_{CC}$ Erase Suspend Current (Block Erase Suspended, $\overline{CS}$ = V$_{IH}$)	I$_{CCES}$		24	40	mA	1,2
V$_{PP}$ Standby/Read Current　　　　　　　　　(V$_{PP}$ ≤ V$_{CC}$) 　　　　　　　　　　　　　　　　　　　(V$_{PP}$ > V$_{CC}$)	I$_{PPS}$ I$_{PPR}$		8 40	60 800	μA	1
V$_{PP}$ Write Current (Word Write in Progress, V$_{PP}$ = V$_{PPH}$)	I$_{PPW}$			160	mA	1,7
V$_{PP}$ Block Erase Current (Block Erase in Progress, V$_{PP}$ = V$_{PPH}$)	I$_{PPE}$			80	mA	1,7
V$_{PP}$ Erase Suspend Current (Block Erase Suspended)	I$_{PPES}$		40	800	μA	1
Input Low Voltage	V$_{IL}$	-0.5		0.8	V	7
Input High Voltage	V$_{IH}$	2.0		V$_{CC}$ +0.5	V	7
Output Low Voltage (I$_{OL}$ =5.8 mA, V$_{CC}$ = V$_{CC}$ Min)	V$_{OL}$			0.45	V	3,7
Output High Voltage　　　　　　(I$_{OH}$ = -2.5mA, V$_{CC}$ = V$_{CC}$ Min) 　　　　　　　　　　　　　　(I$_{OH}$ = -100mA, V$_{CC}$ = V$_{CC}$ Min)	V$_{OH1}$ V$_{OH2}$	0.85 V$_{CC}$ V$_{CC}$ -0.4			V V	3,7
V$_{PP}$ Write/Erase Lock Voltage	V$_{PPLK}$	0.0		1.5	V	4,7
V$_{PP}$ during Write/Erase Operations	V$_{PPH}$	4.5	5.0	5.5	V	
V$_{CC}$ Write/Erase Lock Voltage	V$_{LKO}$	2.0			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V$_{CC}$ = 5.0V, V$_{PP}$ = 12.0V, T = 25°C.
2. I$_{CCES}$ is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I$_{CCES}$ and I$_{CCR}$.
3. Includes RY/$\overline{BY}$.
4. BlockErases, Word Writes and Lock Block operations are inhibited when V$_{PP}$ ≤ V$_{PPLK}$ and not guaranteed in the ranges between V$_{PPLK}$ (max) and V$_{PPH}$ (min), and above V$_{PPH}$ (max).

5. Automatic Power Saving (APS) reduces I$_{CCR}$ to 1mA typical in Static operation.
6. CMOS inputs are either V$_{CC}$ ±0.2V or V$_{SS}$ ±0.2V TTL inputs are either V$_{IL}$ or V$_{IH}$.
7. Sampled, not 100% tested.

AC CHARACTERISTICS - READ-ONLY OPERATIONS[1]

$(V_{CC} = 5.0V \pm 10\%, T_A = -40°C$ to $+85°C)$

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Read cycle time	t_{AVAV}	100			ns	
Address to output delay	t_{AVQV}			100	ns	
$\overline{CS}$ to output delay	t_{ELQV}			100	ns	2
$\overline{RESET}$ to output delay	t_{PHQV}			400	ns	
$\overline{OE}$ to output delay	t_{GLQV}			50	ns	2
$\overline{CS}$ to output in low Z	t_{ELQX}	0			ns	
$\overline{CS}$ to output high Z	t_{EHQZ}			55	ns	
$\overline{OS}$ to output in low Z	t_{GLQX}	0			ns	
$\overline{OE}$ to output high Z	t_{GHQZ}			15	ns	
Output hold from address, $\overline{CS}$ or $\overline{OE}$ change, whichever occurs first	t_{OH}	0			ns	

NOTES:
1. See AC input/output reference waveforms for timing measurements.
2. $\overline{OE}$ may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of $\overline{CS}$, without impacting t_{ELQV}.

AC CHARACTERISTICS - WRITE OPERATION - $\overline{WE}$ CONTROLLED[1, 2]

$(T_A = -40°C$ to $+85°C)$

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{RESET}$ High Recovery to $\overline{WE}$ Going Low	t_{PHWL}	1		µs	3
$\overline{CS}$ Setup to $\overline{WE}$ Going Low	t_{ELWL}	0		ns	5
Write Pulse Width	t_{WP}	50		ns	5
Data Setup to $\overline{WE}$ Going High	t_{DVWH}	40		ns	
Address Setup to $\overline{WE}$ Going High	t_{AVWH}	40		ns	
$\overline{CS}$ Hold from $\overline{WE}$ High	t_{WHEH}	0		ns	
Data Hold from $\overline{WE}$ High	t_{WHDX}	5		ns	
Address Hold from $\overline{WE}$ High	t_{WHAX}	5		ns	
Write Pulse Width High	t_{WPH}	25		ns	6
$\overline{RESET}$ V$_{HH}$ Setup to $\overline{WE}$ Going High	t_{PHHWH}	100		ns	3
V$_{PP}$ Setup to $\overline{WE}$ Going High	t_{VPWH}	100		ns	3
Write Recovery before Read	t_{WHGL}	0		ns	
$\overline{WE}$ High to RY/$\overline{BY}$ Going Low	t_{WHRL}		90	ns	
$\overline{RESET}$ V$_{HH}$ Hold from Valid SRD, RY/$\overline{BY}$ High	t_{QVPH}	0		ns	3,4
V$_{PP}$ Hold from Valid SRD, RY/$\overline{BY}$ High	t_{QVVL}	0		ns	3,4

NOTES:
1. Read timing characteristics during block erase, program, and lock-bit configuration operationsare the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. A write operation can be initiated and terminated with either $\overline{CS}$ or $\overline{WE}$.
3. Guaranteed by design, not 100% tested.
4. V$_{PP}$ should be held at V$_{PPH1/2}$ (and if necessary $\overline{RESET}$ should be held at V$_{HH}$) until determination of block erase, program, or lock-bit configuration success (SR 1/3/4/5 = 0).
5. Write pulse width (t_{WP}) is defined from $\overline{CS}$ or $\overline{WE}$ going low (whichever goes low last) to $\overline{CS}$ or $\overline{WE}$ going high (whichever goes high first). Hence, t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}. If $\overline{CS}$ is driven low 10ns before $\overline{WE}$ going low, $\overline{WE}$ pulse width requirement decreases to t_{WP} -20ns.
6. Write pulse width high (t_{WPH}) is defined from $\overline{CS}$ or $\overline{WE}$ going high (whichever goes high first) to $\overline{CS}$ or $\overline{WE}$ going low (whichever gows low last). Hence, t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}.

AC CHARACTERISTICS - WRITE OPERATION - $\overline{CS}$ CONTROLLED[1, 2]
(T_A = -40°C to +85°C)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{RESET}$ High Recovery to $\overline{CS}$ Going Low	t_{PHEL}	1		µs	3
$\overline{WE}$ Setup to $\overline{CS}$ Going Low	t_{ELEL}	0		ns	5
Data Setup to $\overline{CS}$ Going High	t_{DVEH}	40		ns	
Address Setup to $\overline{CS}$ Going High	t_{AVEH}	40		ns	
$\overline{WE}$ Hold from $\overline{CS}$ High	t_{WHEH}	0		ns	
Data Hold from $\overline{CS}$ High	t_{EHDX}	5		ns	
Address Hold from $\overline{CS}$ High	t_{EHAX}	5		ns	
$\overline{RESET}$ V$_{HH}$ Setup to $\overline{CS}$ Going High	t_{PHHEH}	100		ns	3
V$_{PP}$ Setup to $\overline{CS}$ Going High	t_{VPEH}	100		ns	3
Write Recovery before Read	t_{EHGL}	0		ns	
$\overline{CS}$ High to RY/$\overline{BY}$ Going Low	t_{EHRL}		90	ns	

NOTES:
1. Read timing characteristics during block erase, program, and lock-bit configuration operationsare the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. A write operation can be initiated and terminated with either $\overline{CS}$ or $\overline{WE}$.
3. Guaranteed by design, not 100% tested.
4. V$_{PP}$ should be held at V$_{PPH1/2}$ (and if necessary $\overline{RESET}$ should be held at V$_{HH}$) until determination of block erase, program, or lock-bit configuration success (SR 1/3/4/5 = 0).
5. Write pulse width (t_{WP}) is defined from $\overline{CS}$ or $\overline{WE}$ going low (whichever goes low last) to $\overline{CS}$ or $\overline{WE}$ going high (whichever goes high first). Hence, t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}. If $\overline{CS}$ is driven low 10ns before $\overline{WE}$ going low, $\overline{WE}$ pulse width requirement decreases to t_{WP} -20ns.
6. Write pulse width high (t_{WPH}) is defined from $\overline{CS}$ or $\overline{WE}$ going high (whichever goes high first) to $\overline{CS}$ or $\overline{WE}$ going low (whichever gows low last). Hence, t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}.

BLOCK ERASE, PROGRAM, AND LOCK-BIT CONFIGURATION PERFORMANCE - $\overline{WE}$/$\overline{CS}$ CONTROLLED[3,4,5]

Parameter	Symbol		5V V$_{PP}$			12V V$_{PP}$			Unit	Notes
			Min	Typ	Max	Min	Typ	Max		
Program Time	t_{WHRH1}	t_{EHRH1}	6.5	8	TBD	4.8	6	TBD	µs	2
Block Program Time			0.4	0.5	TBD	0.3	0.4	TBD	sec	2
Block Erase Time	t_{WHRH2}	t_{EHRH2}	0.9	1.1	TBD	0.3	1.0	TBD	sec	2
Set Lock-Bit Time	t_{WHRH3}	t_{EHRH3}	9.5	12	TBD	7.8	10	TBD	µs	2
Clear Block Lock-Bits Time	t_{WHRH4}	t_{EHRH4}	0.9	1.1	TBD	0.3	1.0	TBD	sec	2
Program Suspend Latency Time	t_{WHRH5}	t_{EHRH5}		5	6		4	5	µs	
Erase Suspend Latency Time	t_{WHRH5}	t_{EHRH5}		9.6	12		9.6	12	µs	

NOTES:
1. Typical values measurecd at T_A = +25°C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Guaranteed by design, not 100% tested.
5. Reference the AC waveform for write operations, Fig. 4 and 5.

RESET OPERATIONS

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{RESET}$ Pulse Low Time (If $\overline{RESET}$ is tied to Vcc, this specification is not applicable.)	t_{PLPH}	100		ns	
$\overline{RESET}$ Low to Reset during Block Erase, Program, or Lock-Bit Configuration	t_{PLRH}		12	µs	2

NOTES:
1. These specifications are valid for all product versions (packages and speeds).
2. A reset time, t_{PHQV}, is required from $\overline{RESET}$ going high until outputs are valid.

FIG. 2 AC WAVEFORM FOR $\overline{RESET}$ OPERATION
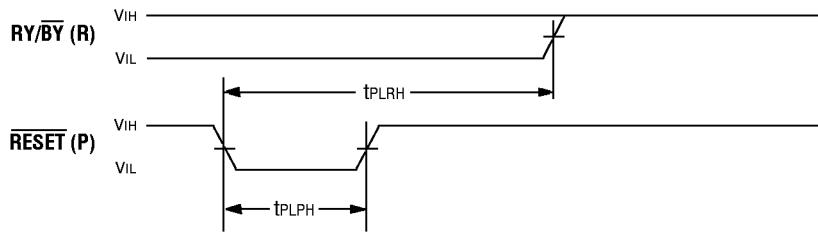
FIG. 3 **AC WAVEFORM FOR READ OPERATIONS**
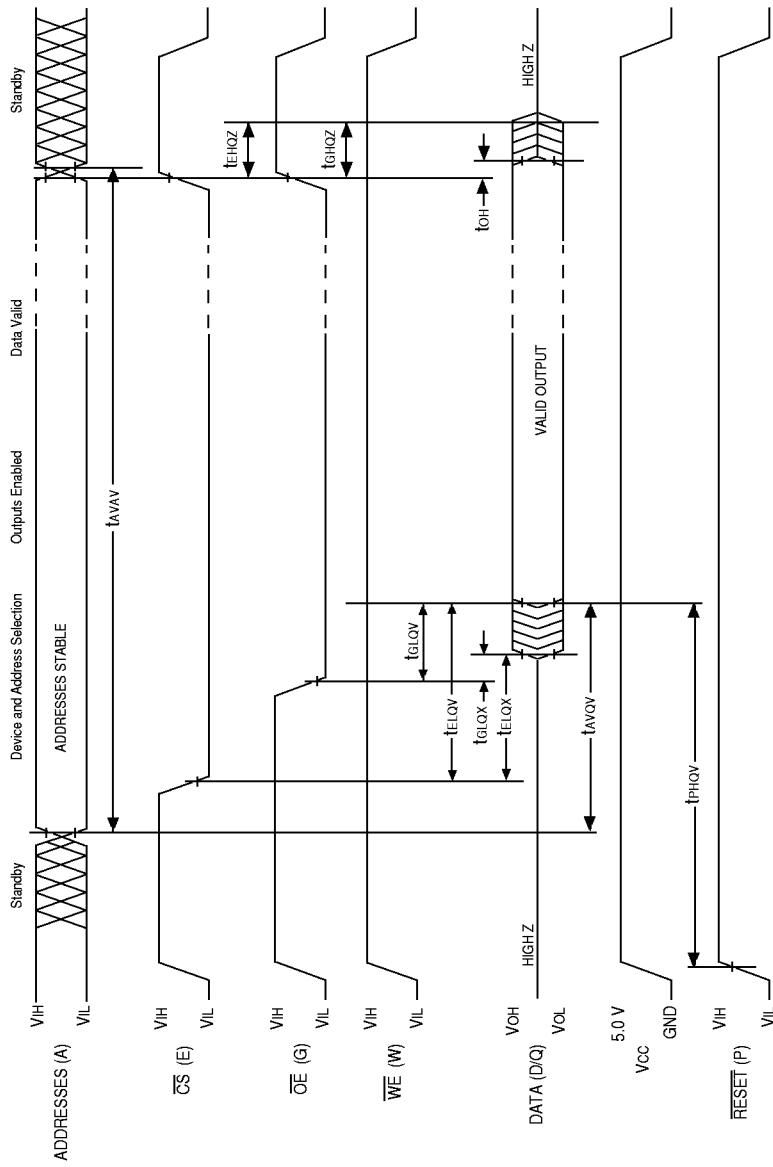
**FIG. 4** AC WAVEFORMS FOR WRITE OPERATIONS - $\overline{WE}$ CONTROLLED
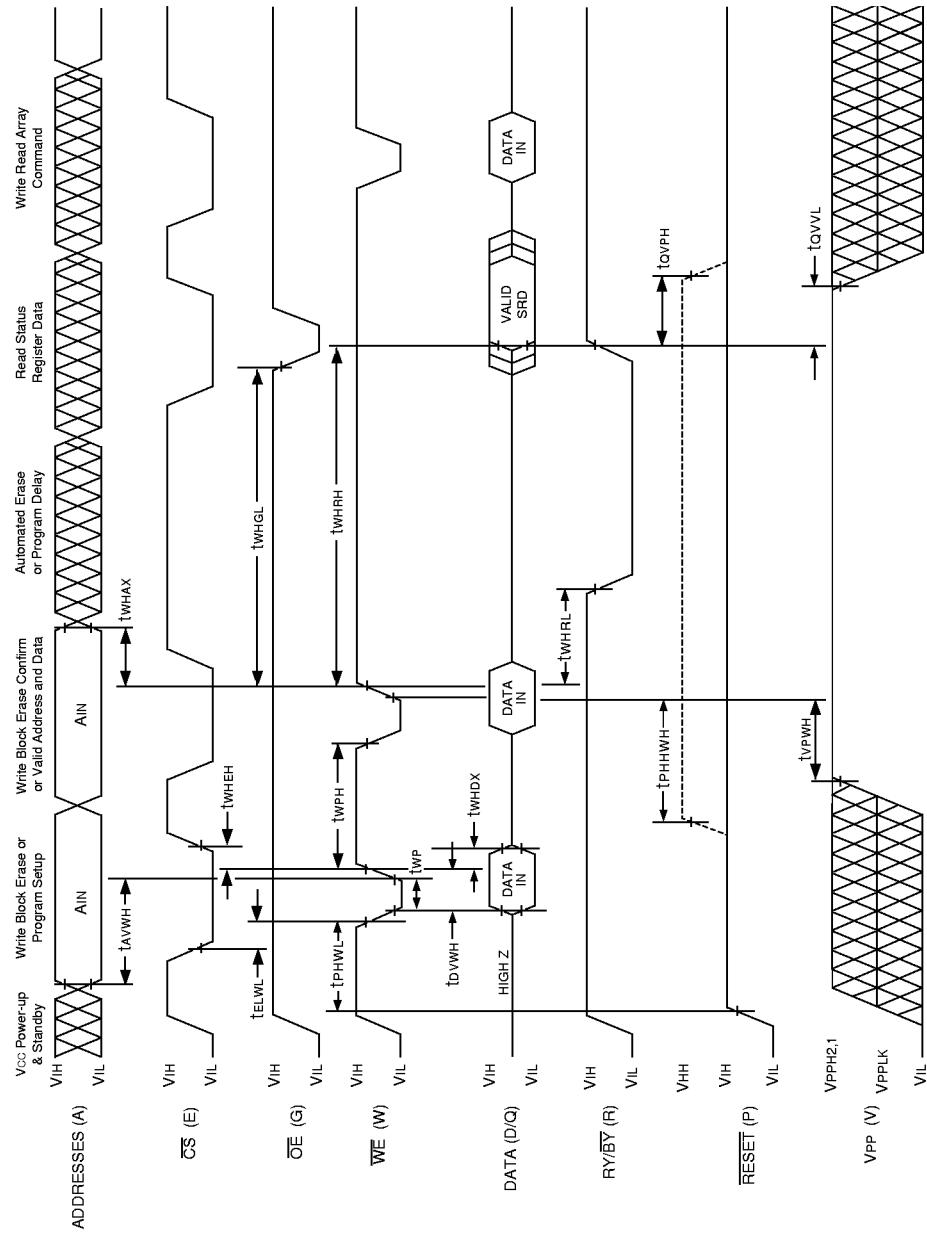
FIG. 5   **ALTERNATE AC WAVEFORM FOR WRITE OPERATIONS - $\overline{CS}$ CONTROLLED**
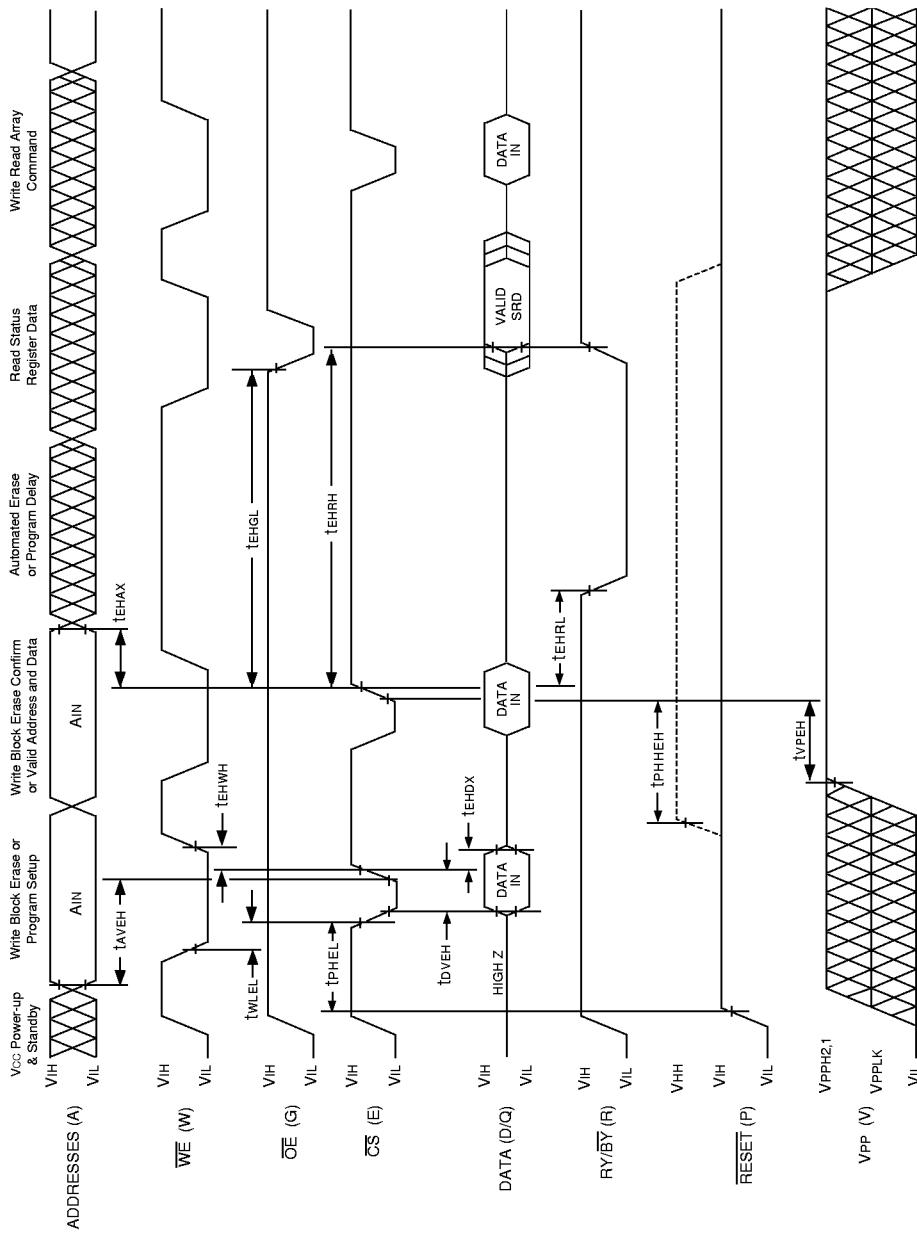
PACKAGE 709: 68 LEAD, PLASTIC PLCC

24.71 (0.973) ± 0.25 (0.010)

4.57 (0.180) MAX

0.46 (0.018) TYP

23.44 (0.923) ± 0.25 (0.010)

1.27 (0.050) TYP
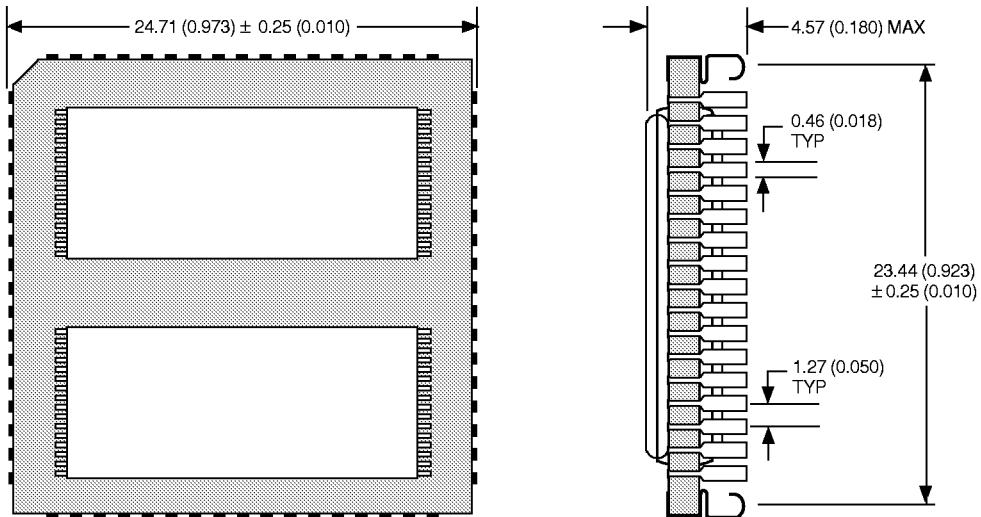
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W P F 2M 32 - 100 PJ X X

Blank = 12V or 5V

DEVICE GRADE:
C = Commercial   0 to +70°C
I = Industrial   -40 to +85°C

PACKAGE TYPE:
PJ = 68 Lead Plastic PLCC (Package 709)

ACCESS TIME (ns)

ORGANIZATION, 2M x 32

Flash PROM

Plastic Multichip Module

WHITE MICROELECTRONICS